REMARKS

In view of the cited art of record, the Applicants submit that all rejections have been overcome and the present application is now in condition for allowance.

Claims 1, 12, 16, 20, 24, and 26 have been amended. Claims 27-33 have been added. Claims 20-26 stand rejected for indefiniteness. Claims 1-26 stand rejected as being anticipated by *Tanaka et al.* (US Pat # 5,559,737), hereinafter "*Tanaka*".

In the Specification

The Specification has been amended such that it is consistent with Fig. 2. The Specification incorrectly referenced the node SINR 246 shown in Fig. 2 as SINB at page 8, line 5.

In the Drawings

The Drawings have not been amended. However, formal drawings are submitted herewith. These formal drawings are believed to address the objections to the drawings. Fig. 3 correctly shows the output of the reference side as RIN 360 and the output of the array side as SIN 370 as stated in the Specification at page 10, lines 17-21. Fig. 3 is consistent with the comments of the Office Action as it stands.

Fig. 4A includes the equalization pulse 410 for illustration purposes only to more easily compare the results between Fig. 4A and 4B. The results shown in Fig. 4A and Fig. 4B both correspond to a FLASH cell programmed to a "one". An equalization pulse was not used to generate the results in Fig. 4A; whereas, an equalization pulse was used to generate the results in Fig. 4B. As such, there is not an extra reference in either Fig. 4A or Fig. 4B.

Fig. 4D includes the equalization pulse 410 for illustration purposes only to more easily compare the results between Fig. 4D and 4C. The results shown in Fig. 4D and Fig. 4C both correspond to a FLASH cell programmed to a "zero". An equalization pulse was not used to generate the results in Fig. 4D; whereas, an equalization pulse was used to generate the results in Fig. 4C.

Claims 20-26 Rejection under 35 U.S.C. § 112

Applicants have amended the claims to more particularly point out and distinctly claim the subject matter which Applicants regard as the invention. The amendments to these claims are believed to render the rejections under 35 U.S.C. § 112 moot.

Claims 1-26 Rejection under 35 U.S.C. § 102(b)

The Office Action rejected all claims as being anticipated by *Tanaka*. *Tanaka* is directed towards an EPROM (Erasable Programmable Read Only Memory) memory and the performance of a high-speed read operation upon the cells of the memory device as stated in the Abstract and at column 9, line 62 to column 10, line 3. As stated in the Abstract, *Tanaka* equalizes the potential between a cell and a dummy cell at two points: 1) between a bit line and a dummy cell bit line and 2) between a sense line and a dummy cell sense line. The gate nodes of two different equalizing N-channel transistors are coupled to a pulse generator as shown in Fig. 2, Fig. 5, and Fig. 11. The first and second nodes of the first equalizing transistor are coupled to the bit line and the dummy cell bit line respectively as also shown in Fig. 2, Fig. 5, and Fig. 11. The first and second nodes of the second equalizing transistor are coupled to the first and second nodes of an equalizing P-channel transistor and to the sense line and the

dummy cell sense line respectively. (*Tanaka*, Fig. 2, Fig. 5, and Fig. 11). The gate node of the equalizing P-channel transistor is coupled to a complementary output pulse from the pulse generator. (*Tanaka*, Fig. 2, Fig. 5, and Fig. 11). Thus, *Tanaka* utilizes 3 equalizing transistors and a pulse generator to generate both a pulse and its complement; whereas, the presently claimed invention utilizes a single equalizing transistor to provide similar performance characteristics as shown by comparing Figures 4A-4B of the present invention and Figures 3, 6, and 12 of *Tanaka*. As a result, the presently claimed invention makes the cited art of *Tanaka* simpler without loss of capability. The independent claims 1, 12, 16, 20, and 24 of the present invention have been amended to include a single equalizing transistor. This important development results in significant savings both in the expense of manufacturing the memory device and in the size of the device. *Tanaka* is further addressed to EPROM type devices as stated from column 9, line 62 to column 10, line 3. The presently claimed invention of Claims 1, 12, 16, and 20 are directed to FLASH memory devices not the EPROM devices referenced by *Tanaka*.

As amended, claims 1, 12, 16, 20, and 24 include an element not found in the cited art. Thus, these claims are ready for allowance. Because all of the remaining claims depend on the now allowable independent claims 1, 12, 16, 20, and 24, these claims also stand ready for allowance.

Claims 27-33 have been added and are supported by the Specification, the Figures, and the claims as originally filed. Again, claims 27-33 reference only a single equalizing transistor. No new matter has been added. Applicant respectfully submits that claims 27-33 are similarly unanticipated by *Tanaka* and are ready for allowance.

Condition for Allowance

Applicants submit that all rejections have been overcome and the present application is now in condition for allowance. If the Examiner has any questions or comments, the Applicants respectfully request that the Examiner contact the undersigned by telephone.

Deposit Account Authorization and Extension of Time Request

Please charge any shortages and credit any overages to Deposit Account No. 02-2666, including any funds necessitated due to insufficient funds for an accompanying check. Any necessary extension of time for response not already requested is hereby requested. Please charge any corresponding fee to Deposit Account No. 02-2666.

Respectfully submitted,

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Date: July 24, 2002

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VERSION WITH MARKINGS TO SHOW CHANGES

IN THE SPECIFICATION

Also coupled to the node SINA 231 is the second node of transistor 228 and the first input of sense amplifier 234. Coupled to the first node of transistor 238 and the first node of transistor 243 is a power supply. Coupled to the gate of transistor 228 and the gate of transistor 243 is current adjust input 240. Coupled to the first node of transistor 243 is node SIN[B]R 246. Node 246 is also coupled to the second input of sense amplifier 234, the first node of transistor 249, the first node of transistor 252, and the second node of transistor 258. The output of sense amplifier 234 is coupled to data 237.

IN THE CLAIMS

1. (Once Amended) An apparatus comprising:

a first drain bias network having an input suitable to couple to a FLASH cell;

a second drain bias network having an input suitable to couple to a FLASH cell; and

an equalization circuit having a first node coupled to the input of the first drain bias network and having a second node coupled to the input of the second drain bias network and having a control signal to control operation of the equalization circuit, wherein the equalization circuit is a single equalizing transistor coupled between the first drain bias network and the second drain bias network.

12. (Once Amended) A method comprising:

equalizing a sense input and a reference input using a single equalizing transistor;

coupling the sense input to a FLASH cell to be sensed;

terminating equalization of the sense input and the reference input; and

measuring a sense voltage, the sense voltage corresponding to the sense input.

16. (Once Amended) An apparatus comprising:

a first bias means for biasing a FLASH cell, the first bias means having an input and an output;

a second bias means for biasing a reference FLASH cell, the second bias means having an input and an output; and

a[n equalization means for selectively equalizing the input of the first bias means and the input of the second bias means, the equalization means] single equalizing transistor having a first node and a second node, the equalizing transistor coupled to the input of the first bias means at the first node and the equalizing transistor coupled to the input of the second bias means at the second node.

20. (Once Amended) A FLASH device comprising:

a FLASH cell array;

a control circuit block coupled to the FLASH cell array to control the FLASH cell array; and

a comparison circuit block coupled to the FLASH cell array and coupled to the control circuit block, the control circuit block to control the comparison circuit, the comparison circuit including:

a first drain bias network having an input suitable to couple to a FLASH cell,

a second drain bias network having an input suitable to couple to a reference FLASH cell, and

an equalization circuit having a first node coupled to the input of the first drain bias network and having a second node coupled to the input of the second drain bias network and having a control signal to control operation of the equalization circuit, wherein the equalization circuit is a single equalizing transistor coupled between the first drain bias network and the second drain bias network.[.]

24. (Once Amended) An apparatus comprising:

a first bias network having an input suitable to couple to a persistent memory storage location;

a second bias network having an input suitable to couple to a reference persistent memory storage location; and

an equalization circuit having a first node coupled to the input of the first bias network and having a second node coupled to the input of the second bias network and having a control signal to control operation of the equalization circuit, wherein the equalization circuit is a single equalizing transistor coupled between the first drain bias network and the second drain bias network.

26. (Once Amended) The apparatus of claim 25 further comprising:

a reference persistent memory storage location coupled to the second bias network through a reference column select circuit and [a] the persistent memory storage location selectively coupled to the first bias network through a column select circuit, the column select circuit controlled by a column select signal.